

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	875	712/225.ccls.	US-PGPUB; USPAT	OR	ON	2009/07/27 17:04
S1	5	(load\$3 with (perform \$3 execut\$3) with background) same thread	US-PGPUB; USPAT	OR	OFF	2004/12/01 14:16
S2	299	(load\$3 near5 inactive) and g06f\$.ipc.	US-PGPUB; USPAT	OR	OFF	2004/12/01 14:17
S3	32	(load\$3 near5 inactive near4 register) and g06f\$.ipc.	US-PGPUB; USPAT	OR	OFF	2004/12/01 14:27
S4	84	"row address registers"	US-PGPUB; USPAT	OR	OFF	2004/12/01 14:27
S5	54	"row address registers" and DRAM	US-PGPUB; USPAT	OR	OFF	2004/12/01 14:32
S6	53	inagami.in.	US-PGPUB; USPAT	OR	OFF	2004/12/01 14:32
S7	2	inagami.in. and mask	US-PGPUB; USPAT	OR	OFF	2004/12/02 08:08
S8	6	(instruction command) with (deactivate de- activate) with row with DRAM	US-PGPUB; USPAT	OR	ON	2004/12/02 08:09
S9	116	(instruction command) with (deactivate de- activate) with (row DRAM)	US-PGPUB; USPAT	OR	ON	2004/12/02 08:12
S10	14	(instruction command) with (deactivate de- activate) with DRAM	US-PGPUB; USPAT	OR	ON	2004/12/02 08:12
S11	1	"5933627".pn.	US-PGPUB; USPAT	OR	OFF	2004/12/02 10:26
S12	41	((functional arithmetic) adj unit) with generat \$3 near3 "memory address"	US-PGPUB; USPAT	OR	ON	2004/12/02 16:50
S13	1	"5,896,523".pn.	US-PGPUB; USPAT	OR	OFF	2004/12/06 14:01
S14	23	dowling-e\$.in. and embedded	US-PGPUB; USPAT	OR	OFF	2004/12/06 14:02

S15	1	(US-20020091916-\$). did.	US-PGPUB	OR	OFF	2004/12/06 14:02
S16	1	S15 and pointer with file	US-PGPUB; USPAT	OR	ON	2004/12/06 14:57
S17	43	"register file" with act \$3 with cache	US-PGPUB; USPAT	OR	ON	2004/12/06 14:58
S18	46	712/5.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/06 16:19
S19	397	712/207.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/06 16:19
S20	137	712/224.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/06 16:19
S21	467	712/225.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/06 16:19
S22	484	712/228.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/06 16:19
S23	166	712/235.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/06 16:19
S24	244	712/237.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/07 10:16
S25	0	dowling-eric.in. and g06f\$.ipc.	US-PGPUB	OR	OFF	2005/07/20 17:23
S26	0	dowling-eric.in.	US-PGPUB	OR	OFF	2005/07/20 17:23
S27	20	dowling-e\$.in.	US-PGPUB	OR	OFF	2005/07/20 17:23
S28	1	(US-20020091916-\$). did.	US-PGPUB	OR	OFF	2005/07/20 17:24
S29	1	S28 and (row with address with register same load\$3 with parallel\$2)	US-PGPUB	OR	ON	2005/07/20 17:25
S30	0	S28 and (DRAM same recharg\$3)	US-PGPUB	OR	ON	2005/07/20 17:25
S31	2486	"active memory"	US-PGPUB; USPAT	OR	ON	2006/03/27 16:50
S32	0	"active memory" same DRAM same processor same embedded	US-PGPUB; USPAT	OR	ON	2006/03/27 16:50
S33	23	"active memory" and DRAM same processor same embedded	US-PGPUB; USPAT	OR	ON	2006/03/27 16:52
S34	402	DRAM with processor with embedded	US-PGPUB; USPAT	OR	ON	2006/03/27 16:52
S35	138	DRAM with processor with embedded with (chip board)	US-PGPUB; USPAT	OR	ON	2006/03/27 16:52

S36	12	(load\$3 with (perform \$3 execut\$3) with background) same thread	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S37	384	(load\$3 near5 inactive) and g06f\$.ipc.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S38	33	(load\$3 near5 inactive near4 register) and g06f\$.ipc.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S39	115	"row address registers"	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S40	69	"row address registers" and DRAM	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S41	53	inagami.in.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S42	2	inagami.in. and mask	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S43	7	(instruction command) with (deactivate deactivate) with row with DRAM	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S44	163	(instruction command) with (deactivate deactivate) with (row DRAM)	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S45	19	(instruction command) with (deactivate deactivate) with DRAM	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S46	1	"5933627".pn.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S47	43	((functional arithmetic) adj unit) with generat \$3 near3 "memory address"	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S48	1	"5,896,523".pn.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S49	43	dowling-e\$.in. and embedded	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S50	0	(US-20020091916-\$). did.	US-PGPUB	OR	OFF	2007/01/17 15:37
S51	0	S50 and pointer with file	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S52	74	"register file" with act \$3 with cache	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S53	62	712/5.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S54	157	712/224.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37

S55	499	712/207.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S56	217	712/235.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S57	292	712/237.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S58	612	712/225.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S59	644	712/228.ccls.	US-PGPUB; USPAT	OR	OFF	2007/01/17 15:37
S60	0	dowling-eric.in. and g06f\$.ipc.	US-PGPUB	OR	OFF	2007/01/17 15:37
S61	0	dowling-eric.in.	US-PGPUB	OR	OFF	2007/01/17 15:37
S62	50	dowling-e\$.in.	US-PGPUB	OR	OFF	2007/01/17 15:37
S63	1	(US-20020091916-\$). did.	US-PGPUB	OR	OFF	2007/01/17 15:37
S64	1	S63 and (row with address with register same load\$3 with parallel\$2)	US-PGPUB	OR	ON	2007/01/17 15:37
S65	0	S63 and (DRAM same recharg\$3)	US-PGPUB	OR	ON	2007/01/17 15:37
S66	2775	"active memory"	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S67	0	"active memory" same DRAM same processor same embedded	US-PGPUB; USPAT	OR	ON	2007/01/17 15:40
S68	24	"active memory" and DRAM same processor same embedded	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S69	454	DRAM with processor with embedded	US-PGPUB; USPAT	OR	ON	2007/01/17 15:37
S70	152	DRAM with processor with embedded with (chip board)	US-PGPUB; USPAT	OR	ON	2007/01/17 15:40
S72	0	"active memory" same DRAM same processor same embedded	US-PGPUB; USPAT; USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/17 15:40
S73	13	DRAM with processor with embedded with (chip board)	USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/27 14:24

S74	472	(DRAM RAM "dynamic random") with (microprocessor processor CPU) with (integrated embedded single) near3 (chip IC "integrated circuit")	USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/27 14:27
S75	224	(DRAM "dynamic random") with (microprocessor processor CPU) with (integrated embedded single) near3 (chip IC "integrated circuit")	USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/27 14:27
S76	1430	(DRAM "dynamic random") with (microprocessor processor CPU) with (integrated embedded single) near3 (chip IC "integrated circuit")	US-PGPUB; USPAT; USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/27 14:27
S77	440	(DRAM "dynamic random") near5 (microprocessor processor CPU) near3 (integrated embedded single) near3 (chip IC "integrated circuit")	US-PGPUB; USPAT; USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/27 14:29
S78	374	(DRAM "dynamic random") near5 (microprocessor processor CPU) near3 (integrated embedded single) near3 (chip IC "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/07/27 14:51
S79	0	dowling-eric.in. and hewlett.as.	US-PGPUB; USPAT	OR	ON	2007/07/27 14:51
S80	0	dowling-eric.in.	US-PGPUB; USPAT	OR	ON	2007/07/27 14:51
S81	107	dowling-eri\$.in.	US-PGPUB; USPAT	OR	ON	2007/07/27 14:52
S82	211	(instruction command) near4 (precharge\$3 pre-charge\$3) near4 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 14:59

S83	0	explicit\$3 with (instruction command) near4 (precharg\$3 precharg\$3) near4 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 14:59
S84	211	(instruction command) near4 (precharg\$3 precharg\$3) near4 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 15:00
S85	5	(instruction command) near4 (precharg\$3 precharg\$3) near4 (DRAM "dynamic random access memory") and (instruction command) near4 (deactivat\$3 deactivat\$3) near4 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 15:11
S86	15	(instruction command) near4 (deactivat\$3 deactivat\$3) near4 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 15:17
S87	510	(instruction command) near4 (refresh\$3 disabl\$3 inhibit\$3 prohibit\$3) near4 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 15:17
S88	413	(instruction command) near3 (refresh\$3 disabl\$3 inhibit\$3 prohibit\$3) near3 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 15:20
S89	411	(instruction command) near3 (refresh\$3 disabl\$3) near3 (DRAM "dynamic random access memory")	US-PGPUB; USPAT	OR	ON	2007/07/27 15:38
S90	22	DRAM with inaccessible with refresh\$3	US-PGPUB; USPAT	OR	ON	2007/07/27 15:38
S91	0	DRAM with refresh\$3 with "cannot be accessed"	US-PGPUB; USPAT	OR	ON	2007/07/27 15:41

S92	3758	DRAM with refresh\$3 with access\$3	US-PGPUB; USPAT	OR	ON	2007/07/27 15:42
S93	5	DRAM with refresh\$3 with respond\$3 with (load read)	US-PGPUB; USPAT	OR	ON	2007/07/27 15:43
S94	60	huisman.xa.	US-PGPUB; USPAT	OR	ON	2007/07/27 18:02
S95	23	predict\$3 with load same prefetch\$3 same count\$2	US-PGPUB; USPAT	OR	ON	2008/01/10 13:14
S96	65637	"huisman."(xa xp)". and (employ\$3 with cache with hit).clm.	US-PGPUB; USPAT	OR	ON	2008/04/15 14:19
S97	2	(huisman.xa. hui sman.xp.) and (employ\$3 with cache with hit).clm.	US-PGPUB; USPAT	OR	ON	2008/04/15 14:19
S98	25	predict\$3 with load same prefetch\$3 same count\$2	US-PGPUB; USPAT	OR	ON	2008/04/15 15:54
S99	9	(instruction command) near3 (disable deactivate) with "register file"	US-PGPUB; USPAT	OR	ON	2009/01/15 16:54
S100	1	(instruction command) near3 (disable deactivate) with "register file"	USOCR; FFRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 16:56
S101	31	"thread switch instruction"	US-PGPUB; USPAT	OR	ON	2009/01/15 16:59
S102	11	explicit near2 (context thread) near2 switch	US-PGPUB; USPAT	OR	ON	2009/01/15 17:00
S103	2	("6314510" "6401155").pn.	US-PGPUB; USPAT	OR	ON	2009/01/15 17:03

EAST Search History (I interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	66	(plurality multiple (first and second)) adj "instruction set" same register same (DRAM memory RAM)	USPAT; UPAD	OR	ON	2009/07/27 17:08

L4	31	(plurality multiple (first and second)) adj "instruction set" and (plurality multiple (first and second)) adj "register file" and (DRAM memory RAM)	USPAT; UPAD	OR	ON	2009/07/27 17:10
L5	31	(plurality multiple (first and second)) adj "instruction sets" and (plurality multiple (first and second)) adj "register file" and (DRAM memory RAM)	USPAT; UPAD	OR	ON	2009/07/27 17:21
L6	8	(plurality multiple (first and second)) adj instruction adj sets! and (plurality multiple (first and second)) adj "register file" and (DRAM memory RAM)	USPAT; UPAD	OR	ON	2009/07/27 17:22

7/27/09 5:36:25 PM

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